AMD UMA/PX Schematics

AMD Gardenia 15h 16h FP4 Package

AMD Geo GPU Family Exo Pro S3 Package

SB

APM	APM-69
Functional Data sheet	53556
EDS	53083
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Exo Databook	54766
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VDDCR_CPU	1V_CPU_CORE
VDDCR_NB	APU_VDDNB
VDDCR_GFX	VDDGFX_CORE
VDDIO_MEM_S3	1D35V_CPU_VDDQ_S3
VDDP	0D95V_S0
VDDP_GFX	0D95V_GFX_S0
VDDP_S5	0D95V_S5
VDD18	1D8V_S0
VDD_18_S5	1D8V_S5
VDD_33	3D3V_S0
VDD_33_S5	3D3V_S5
VDDIO_AUDIO	1D5V_S0
VDDBT_RTC_G	1P5V_LPS_APU

The definition of Property:

CZ: Carrizo
- **AMD Family 15h Models 60h-6Fh Processor (BKDG)**
- **AMD FP4 APU (Functional Datasheet)**

CZ: Carrizo-L
- **AMD Family 16h Models 30h-3Fh Processor (BKDG)**
- **AMD FP4 APU (Functional Datasheet)**

PWR CZ: for external "1D2V_GFX_CORE" power.
CZ ->Mount
CZL->Unmount
EXO: Mount for EXO GPU
MESO: Mount for MESO GPU
PX PEG CZ/CZL: Mount for CZ+EXO GPU,it's for DIG,not UMA
PX PEG CZ: Mount for CZ CPU+MESO GPU for DIG,no UMA
DP SW: mount it and it's for DP switch(DVI to VGA/HDMI)
Non-DP SW: Unmount if there is no DP switch
DP SW_I2C:DP switch IIC mode.
DP SW_Pin: DP switch Pin mode
IOAC: There is IOAC function
NON-IOAC: There is no IOAC function
TS_I2C_CZ: Touch panel IIC mode for CZ.
TS_I2C_CZL: Touch panel IIC mode for CZL.
TS_USB_CZ: Touch panel connects to CZ processor.
TPM: Mount it if there is TPM function.
DC PERTECT: just for CZ processor+ MESO GPU.
LPC: OP MODE
LAB: for LAB debug
DY: Unmount
ZZ : Remove

CZL MUA 455.04Z01.M018

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Title: ***Cover Page***

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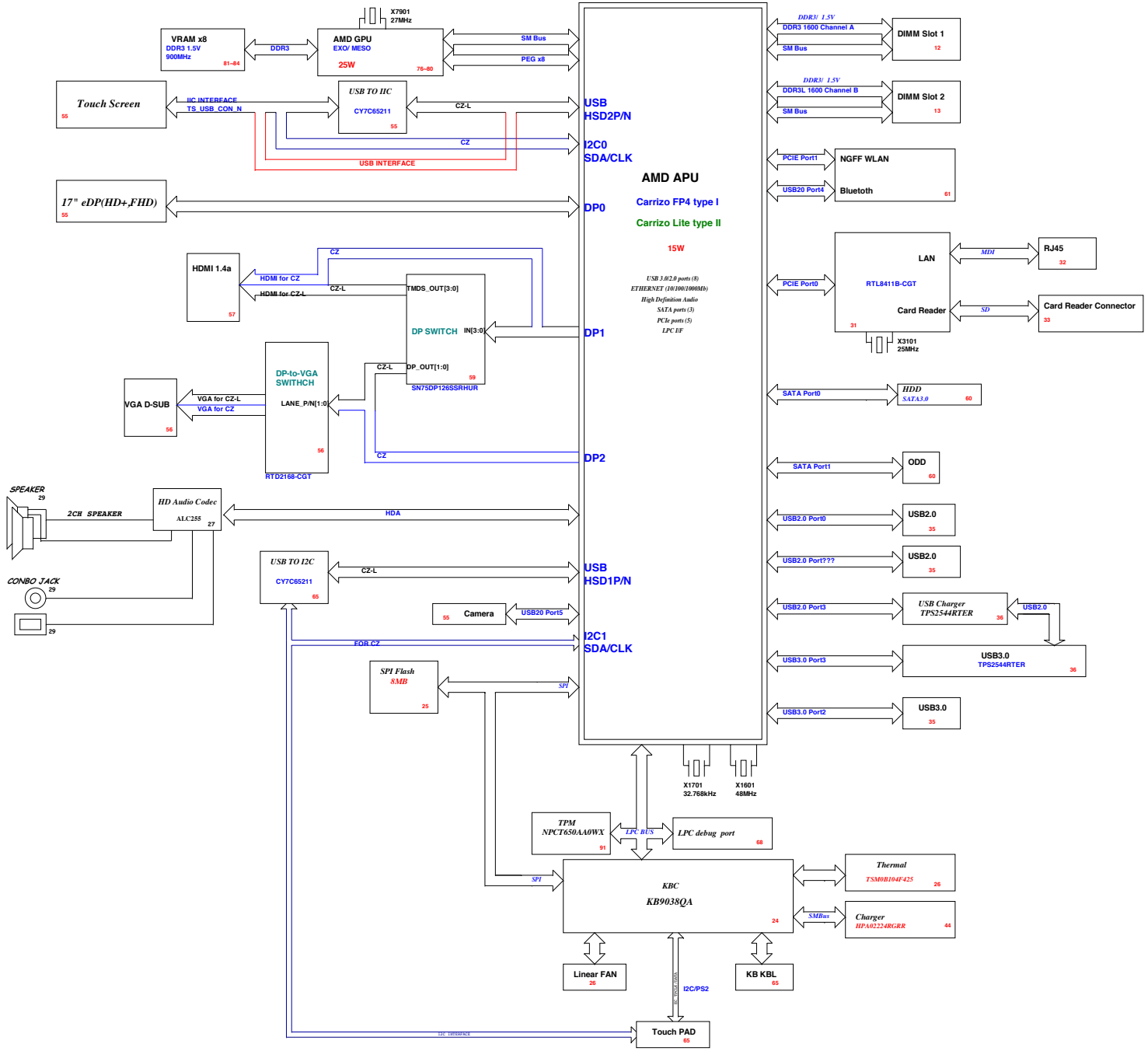
Board Block Diagram



LT415L LT415C	4PD03N010001
LC415L LC415C	4PD03R010001
LC515L LC515C	4PD03S010001
Main Board	14235
IO Board	14882
GSensor + Hall Sensor BD	14875
Hall Sensor Board	14876

CHARGER HPA02224RGRR 44	
INPUTS	OUTPUTS
19V_DCBATOUT	BT+
SYSTEM DC/DC RT6575BGQW 45	
INPUTS	OUTPUTS
19V_DCBATOUT	5V_S5 3D3V_S5
CPU DC/DC RT8179CGQW 46-48	
INPUTS	OUTPUTS
19V_DCBATOUT	1V_CPU_CORE APU_VDDNB
CPU DC/DC RT8179CGQW 49-50	
INPUTS	OUTPUTS
19V_DCBATOUT	VDDGFX_CORE
SYSTEM DC/DC APL5337KAI 50	
INPUTS	OUTPUTS
1D8V_S5	0D775V_S5
SYSTEM DC/DC TPS51716RUKR	
INPUTS	OUTPUTS
19V_DCBATOUT	1D35V_CPU_VDDQ_S3 0D675V_S0
SYSTEM DC/DC AOZ1268QI 51	
INPUTS	OUTPUTS
19V_DCBATOUT	0D95V_S5
SYSTEM DC/DC RT8509GQW 53	
INPUTS	OUTPUTS
5V_S0	15V_LCD
SYSTEM DC/DC ISL62771HRTZ-T 85	
INPUTS	OUTPUTS
19V_DCBATOUT	1V_VGACORE_S0
Switches 40 86	
INPUTS	OUTPUTS
APU_VDDNB 0D775V_S5 3D3V_S0 1D8V_S0 0D95V_S0 1D35V_CPU_VDDQ_S3	VDDCR_FCH_S5 3D3V_VGA_S0 1D8V_VGA_S0 0D95V_VGA_S0 1D35V_VGA_S0
PCBA Layer	L1 TOP L4 Signal L2 VCC L5 GND L3 Signal L6 Bottom

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Title: Block Diagram

Size: M | Document Number: Franky_CZ/CZ-L | Rev: -3

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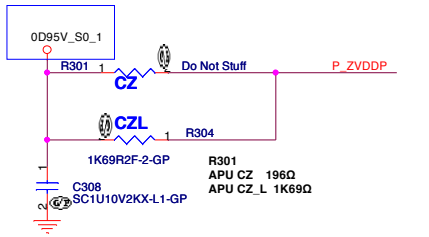
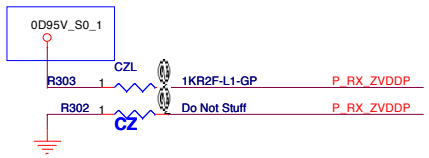
PCIe

P_GPP CLK port	Device	CLKREQ#
0	LAN+CR	0
1	WIFI	1
2		2
3		3

20141208 SB



20141208 SB



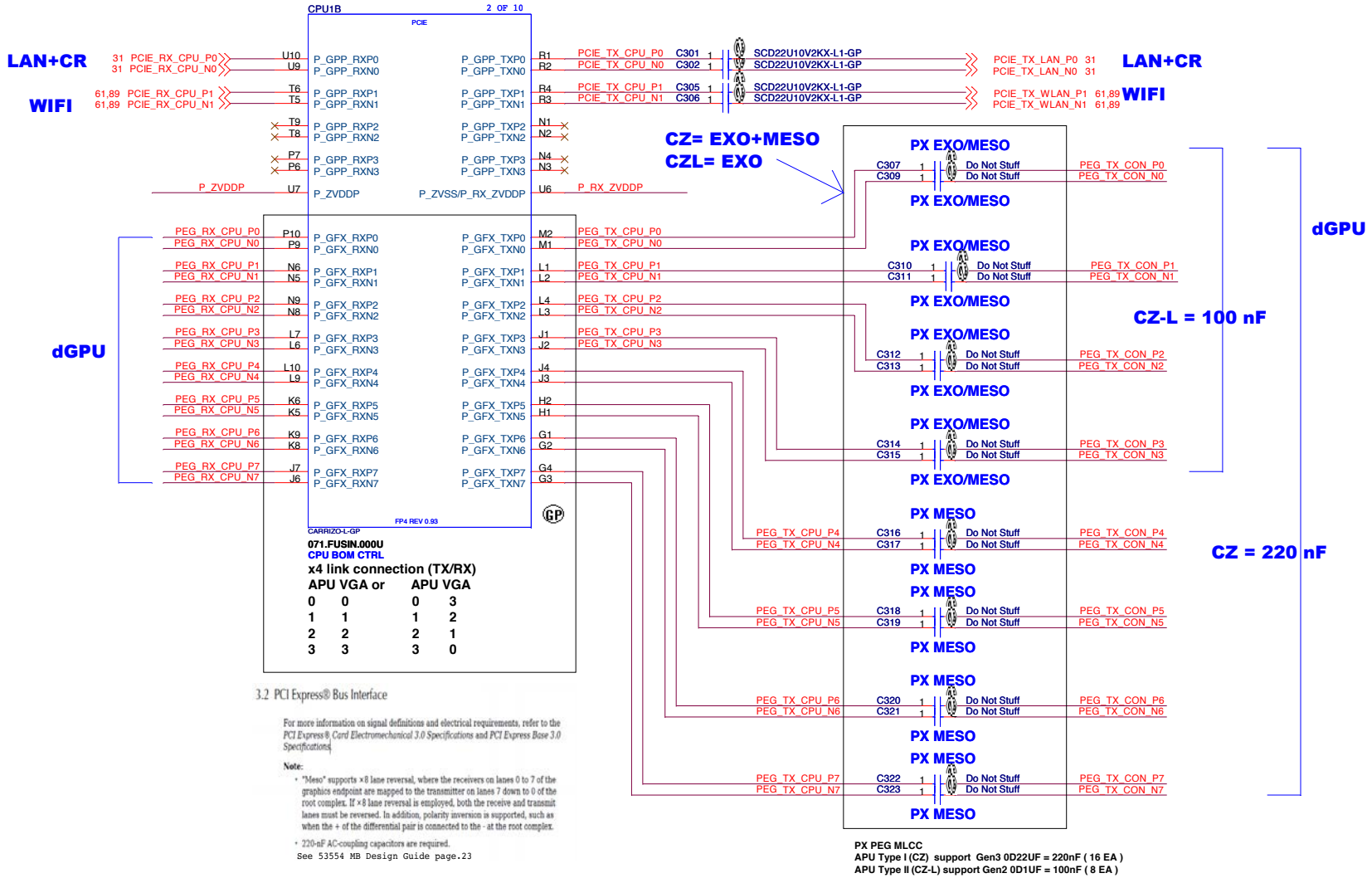
76 PEG_TX_CON_P[0..7]
PEG_TX_CON_P0
PEG_TX_CON_P1
PEG_TX_CON_P2
PEG_TX_CON_P3
PEG_TX_CON_P4
PEG_TX_CON_P5
PEG_TX_CON_P6
PEG_TX_CON_P7

76 PEG_TX_CON_N[0..7]
PEG_TX_CON_N0
PEG_TX_CON_N1
PEG_TX_CON_N2
PEG_TX_CON_N3
PEG_TX_CON_N4
PEG_TX_CON_N5
PEG_TX_CON_N6
PEG_TX_CON_N7

76 PEG_RX_CPU_P[0..7]
PEG_RX_CPU_P0
PEG_RX_CPU_P1
PEG_RX_CPU_P2
PEG_RX_CPU_P3
PEG_RX_CPU_P4
PEG_RX_CPU_P5
PEG_RX_CPU_P6
PEG_RX_CPU_P7

76 PEG_RX_CPU_N[0..7]
PEG_RX_CPU_N0
PEG_RX_CPU_N1
PEG_RX_CPU_N2
PEG_RX_CPU_N3
PEG_RX_CPU_N4
PEG_RX_CPU_N5
PEG_RX_CPU_N6
PEG_RX_CPU_N7

GFX & GPP, 85Ω



x4 link connection (TX/RX)

APU VGA or		APU VGA	
0	0	0	3
1	1	1	2
2	2	2	1
3	3	3	0

PX PEG MLCC
APU Type I (CZ) support Gen3 0D22UF = 220nF (16 EA)
APU Type II (CZ-L) support Gen2 0D1UF = 100nF (8 EA)

3.2 PCI Express® Bus Interface

For more information on signal definitions and electrical requirements, refer to the *PCI Express® Card Electromechanical 3.0 Specifications* and *PCI Express Base 3.0 Specifications*.

Note:

- "Meso" supports ×8 lane reversal, where the receivers on lanes 0 to 7 of the graphics endpoint are mapped to the transmitter on lanes 7 down to 0 of the root complex. If ×8 lane reversal is employed, both the receive and transmit lanes must be reversed. In addition, polarity inversion is supported, such as when the + of the differential pair is connected to the - at the root complex.
- 220-nF AC-coupling capacitors are required.

See 53554 MB Design Guide page.23

3.5 AMD Carrizo & Carrizo-L

AMD Carrizo	AMD Carrizo-L	Acer 2015
PCIe Port0	PCIe Port0	LAN + CR
PCIe Port1	PCIe Port1	WiFi
PCIe Port2	PCIe Port2	M.2 SSD (PCIeX2)
PCIe Port3	PCIe Port3	
SATA0	SATA0	HDD
SATA1	SATA1	ODD
USB2 Port0	USB2 Port0	USB 2 (I/O)
USB2 Port1	USB2 Port1	PTP
USB2 Port2	USB2 Port2	TS
USB2 Port3	USB2 Port3	CR (USB) / FP / Sensor Hub
USB2 Port4 / USB3 Port0	USB2 Port4	BT
USB2 Port5 / USB3 Port1	USB2 Port5	CCD
USB2 Port6 / USB3 Port2	USB2 Port6 / USB3 Port2	USB 3 (I/O)
USB2 Port7 / USB3 Port3	USB2 Port7 / USB3 Port3	USB 3 (I/O)
PEG Port0	PEG Port0	
PEG Port1	PEG Port1	
PEG Port2	PEG Port2	
PEG Port3	PEG Port3	
PEG Port4	N/A	
PEG Port5	N/A	
PEG Port6	N/A	
PEG Port7	N/A	dGPU

Table 48. Component Table—PCIe® to Connector

Ref	Value[1,2]	Tolerance	Package	Placement Location
$C_{Coupling}$	PCIe® Gen3 Allowable Range: 176 to 265 nF Recommended Value: 220 nF PCIe Gen2 Allowable Range: 75 to 200 nF Recommended Value: 100 nF	10%	0402	Place as pairs[3,4]

Note:
1. Capacitor material is X5R.
2. When both Gen2 and Gen3 devices will be supported use the Gen3 recommended value of 220 nF.
3. Placing capacitors as pairs requires traces to be length matched.
4. The AC-coupling capacitors for each pair should be placed as a pair within 0.889 mm of each other. See PCIe AC-Coupling Capacitors for more details.

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Title: **FP4_PCIE**

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DDR3

APU Type 2 does not support Channel A

1D5V_CPU_VDDQ_S3 — R504 1 — CZ — Do Not Stuff — M_A_ZVDDIO

ADD, CMD, CTL, 40Ω
DQ, 50Ω
Misc. 40~60Ω
DDR CLK, 72Ω
DQS, 80Ω

M_VREF
MA_VREFDQ, MB_VREFDQ

1D5V_CPU_VDDQ_S3 — R505 1KR2F-L1-GP — R507 1KR2F-L1-GP — C501 SCD1U16V2KX-L-GP — M_VREF — C502 Do Not Stuff DY — C503 SCD1U16V2KX-L-GP

20150117 -1

ADD and CLK on the sam layer

CPU1A — 1 OF 10 — MEMORY A

12 M_A_A[15..0]

M_A_A0	AE28	MA_ADD0
M_A_A1	Y27	MA_ADD1
M_A_A2	Y29	MA_ADD2
M_A_A3	Y26	MA_ADD3
M_A_A4	W28	MA_ADD4
M_A_A5	W29	MA_ADD5
M_A_A6	W26	MA_ADD6
M_A_A7	U29	MA_ADD7
M_A_A8	W25	MA_ADD8
M_A_A9	U26	MA_ADD9
M_A_A10	AG29	MA_ADD10
M_A_A11	U27	MA_ADD11
M_A_A12	T28	MA_ADD12
M_A_A13	AK26	MA_ADD13
M_A_A14	T26	MA_ADD14/MA_BG1
M_A_A15	T25	MA_ADD15/MA_ACT_L

12 M_A_BS[2..0]

M_A_BS0	AG26	MA_BANK0
M_A_BS1	AG27	MA_BANK1
M_A_BS2	T29	MA_BANK2/MA_BG0

12 M_A_DM[7..0]

M_A_DM0	E19	MA_DM0
M_A_DM1	D21	MA_DM1
M_A_DM2	K21	MA_DM2
M_A_DM3	F29	MA_DM3
M_A_DM4	AP28	MA_DM4
M_A_DM5	AV26	MA_DM5
M_A_DM6	AR22	MA_DM6
M_A_DM7	BC22	MA_DM7
ECC support	K29	MA_DM8

DM, DQ & DQS on the same layer

12 M_A_DQS_DP[7..0]

M_A_DQS_DP0	H19	MA_DQS_H0
M_A_DQS_DP1	B22	MA_DQS_L0
M_A_DQS_DP2	A22	MA_DQS_H1
M_A_DQS_DP3	F23	MA_DQS_L1
M_A_DQS_DP4	E23	MA_DQS_H2
M_A_DQS_DP5	G27	MA_DQS_L2
M_A_DQS_DP6	F27	MA_DQS_H3
M_A_DQS_DP7	AP25	MA_DQS_L3

12 M_A_DQS_DN[7..0]

M_A_DQS_DN0	G19	MA_DQS_H4
M_A_DQS_DN1	A22	MA_DQS_L4
M_A_DQS_DN2	F23	MA_DQS_H5
M_A_DQS_DN3	G27	MA_DQS_L5
M_A_DQS_DN4	AP26	MA_DQS_H6
M_A_DQS_DN5	AW27	MA_DQS_L6
M_A_DQS_DN6	AV22	MA_DQS_H7
M_A_DQS_DN7	AU22	MA_DQS_L7
ECC support	BA21	MA_DQS_H8
ECC support	AY21	MA_DQS_L8

DM, DQ & DQS on the same layer

12 M_A_DQ[63..0]

H17	M_A_DQ0	MA_DATA0
J17	M_A_DQ1	MA_DATA1
F20	M_A_DQ2	MA_DATA2
H20	M_A_DQ3	MA_DATA3
E17	M_A_DQ4	MA_DATA4
F17	M_A_DQ5	MA_DATA5
K18	M_A_DQ6	MA_DATA6
E20	M_A_DQ7	MA_DATA7
A21	M_A_DQ8	MA_DATA8
C21	M_A_DQ9	MA_DATA9
C23	M_A_DQ10	MA_DATA10
D23	M_A_DQ11	MA_DATA11
B20	M_A_DQ12	MA_DATA12
B21	M_A_DQ13	MA_DATA13
B23	M_A_DQ14	MA_DATA14
A23	M_A_DQ15	MA_DATA15
G22	M_A_DQ16	MA_DATA16
H22	M_A_DQ17	MA_DATA17
E25	M_A_DQ18	MA_DATA18
G25	M_A_DQ19	MA_DATA19
J20	M_A_DQ20	MA_DATA20
E22	M_A_DQ21	MA_DATA21
H23	M_A_DQ22	MA_DATA22
J23	M_A_DQ23	MA_DATA23
F26	M_A_DQ24	MA_DATA24
E27	M_A_DQ25	MA_DATA25
J26	M_A_DQ26	MA_DATA26
J27	M_A_DQ27	MA_DATA27
H25	M_A_DQ28	MA_DATA28
E26	M_A_DQ29	MA_DATA29
G28	M_A_DQ30	MA_DATA30
G29	M_A_DQ31	MA_DATA31
AN26	M_A_DQ32	MA_DATA32
AP29	M_A_DQ33	MA_DATA33
AR26	M_A_DQ34	MA_DATA34
AP24	M_A_DQ35	MA_DATA35
AN29	M_A_DQ36	MA_DATA36
AN27	M_A_DQ37	MA_DATA37
AR29	M_A_DQ38	MA_DATA38
AR27	M_A_DQ39	MA_DATA39
AU26	M_A_DQ40	MA_DATA40
AV29	M_A_DQ41	MA_DATA41
AU25	M_A_DQ42	MA_DATA42
AW25	M_A_DQ43	MA_DATA43
AU29	M_A_DQ44	MA_DATA44
AU28	M_A_DQ45	MA_DATA45
AW26	M_A_DQ46	MA_DATA46
AT25	M_A_DQ47	MA_DATA47
AV23	M_A_DQ48	MA_DATA48
AW23	M_A_DQ49	MA_DATA49
AV20	M_A_DQ50	MA_DATA50
AW20	M_A_DQ51	MA_DATA51
AR23	M_A_DQ52	MA_DATA52
AT23	M_A_DQ53	MA_DATA53
AR20	M_A_DQ54	MA_DATA54
AT20	M_A_DQ55	MA_DATA55
BB23	M_A_DQ56	MA_DATA56
BB22	M_A_DQ57	MA_DATA57
BB20	M_A_DQ58	MA_DATA58
AY19	M_A_DQ59	MA_DATA59
BA23	M_A_DQ60	MA_DATA60
BC23	M_A_DQ61	MA_DATA61
BC21	M_A_DQ62	MA_DATA62
BB21	M_A_DQ63	MA_DATA63

20150317 -2

SM_A_DRAMRST# — ED501 — Do Not Stuff — CZ

12 M_A_CLK0 — AE25 — MA_CLK_H0
12 M_A_CLK#0 — AE26 — MA_CLK_L0
12 M_A_CLK1 — AD26 — MA_CLK_H1
12 M_A_CLK#1 — AD27 — MA_CLK_L1
AB28 — MA_CLK_H2
AB29 — MA_CLK_L2
AB25 — MA_CLK_H3
AB26 — MA_CLK_L3

1D5V_CPU_VDDQ_S3 — R502 1 — 1KR2J-L2-GP

12 SM_A_DRAMRST# — N29 — MA_RESET_L
12 M_A_EVENT# — AE29 — MA_EVENT_L

12 M_A_CKE0 — P27 — MA_CKE0
12 M_A_CKE1 — P29 — MA_CKE1

For a one DIMM configuration use either M0_xx or M1_xx for these two signal groups only. Must use the same (M0 or M1) group for both CS and ODT.

12 M_A_ODT0 — AK27 — MA0_ODT0
12 M_A_ODT1 — AL26 — MA0_ODT1
AH25 — MA1_ODT0
AL25 — MA1_ODT1

12 M_A_CS#0 — AH26 — MA0_CS_L0
12 M_A_CS#1 — AL29 — MA0_CS_L1
AH29 — MA1_CS_L0
AL28 — MA1_CS_L1

12 M_A_RAS# — AG24 — MA_RAS_L/MA_RAS_L_ADD16
12 M_A_CAS# — AK29 — MA_CAS_L/MA_CAS_L_ADD15
12 M_A_WE# — AH28 — MA_WE_L/MA_WE_L_ADD14

M_VREF — B19 — MA_VREFDQ
T32 — M_VREF

MA_ZVDDIO_MEM_S — AD29 — M_A_ZVDDIO

FP4 REV 0.93

CARRIZO-L-GP
071.FUSIN.000U
CPU BOM CTRL

ECC support
MB_CHECK[7:0]
MB_DQS_H/L[8]
MB_DM[8]

MA_CHECK0	K26
MA_CHECK1	K28
MA_CHECK2	N26
MA_CHECK3	N28
MA_CHECK4	J29
MA_CHECK5	K25
MA_CHECK6	L29
MA_CHECK7	N25

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Title: FP4_DDRIII_CHA
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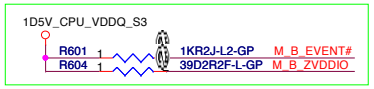
DDR3



Signal GRP	Signal			
Clocks	CLK			
Address	ADD	BANK		
Command	RAS_L	CAS_L	WE_L	
Control	CKE	ODT	CS_L	
Data	Data	CHECK	DM	DQS
Misc.	M_RESET_L	M_EVENT_L		

ADD, CMD, CTL, 40Ω
DQ, 50Ω
Misc. 40~60Ω
DDR CLK, 72Ω
DQS, 80Ω

ADD and CLK on the sam layer

DM, DQ & DQS on the same layer

CPU1I — 9 OF 10 — MEMORY B

13 M_B_A[15..0]

M_B_A0	AG31	MB_ADD0
M_B_A1	AC30	MB_ADD1
M_B_A2	AC31	MB_ADD2
M_B_A3	AB32	MB_ADD3
M_B_A4	AA32	MB_ADD4
M_B_A5	AA33	MB_ADD5
M_B_A6	AA31	MB_ADD6
M_B_A7	Y33	MB_ADD7
M_B_A8	AA30	MB_ADD8
M_B_A9	W32	MB_ADD9
M_B_A10	AG32	MB_ADD10
M_B_A11	Y32	MB_ADD11
M_B_A12	W33	MB_ADD12
M_B_A13	AL31	MB_ADD13
M_B_A14	W30	MB_ADD14/MB_BG1
M_B_A15	V32	MB_ADD15/MB_ACT_L

13 M_B_BS[2..0]

M_B_BS0	AH32	MB_BANK0
M_B_BS1	AG33	MB_BANK1
M_B_BS2	W31	MB_BANK2/MB_BG0

13 M_B_DM[7..0]

M_B_DM0	D25	MB_DM0
M_B_DM1	D29	MB_DM1
M_B_DM2	E33	MB_DM2
M_B_DM3	J33	MB_DM3
M_B_DM4	AR30	MB_DM4
M_B_DM5	AW30	MB_DM5
M_B_DM6	BC30	MB_DM6
M_B_DM7	BC26	MB_DM7
ECC support	N33	MB_DM8

13 M_B_DQS_DP[7..0]

M_B_DQS_DP0	B26	MB_DQS_H0
M_B_DQS_DP1	B30	MB_DQS_L0
M_B_DQS_DP2	F32	MB_DQS_H1
M_B_DQS_DP3	K32	MB_DQS_L1
M_B_DQS_DP4	AR32	MB_DQS_H2
M_B_DQS_DP5	AW32	MB_DQS_L2
M_B_DQS_DP6	BA29	MB_DQS_H3
M_B_DQS_DP7	BA25	MB_DQS_L3
ECC support	P32	MB_DQS_H4

13 M_B_DQS_DN[7..0]

M_B_DQS_DN0	A26	MB_DQS_L4
M_B_DQS_DN1	A30	MB_DQS_H5
M_B_DQS_DN2	E32	MB_DQS_L5
M_B_DQS_DN3	J32	MB_DQS_H6
M_B_DQS_DN4	AR33	MB_DQS_L6
M_B_DQS_DN5	AW33	MB_DQS_H7
M_B_DQS_DN6	AY29	MB_DQS_L7
M_B_DQS_DN7	AY25	MB_DQS_H8
ECC support	N32	MB_DQS_L8

13 M_B_CLK0 — AE33 — MB_CLK_H0
13 M_B_CLK#0 — AE32 — MB_CLK_L0
13 M_B_CLK1 — AE30 — MB_CLK_H1
13 M_B_CLK#1 — AE31 — MB_CLK_L1
AD32 — MB_CLK_H2
AD33 — MB_CLK_L2
AC33 — MB_CLK_H3
AC32 — MB_CLK_L3

13 SM_B_DRAMRST# — T33 — MB_RESET_L
13 M_B_EVENT# — AG30 — MB_EVENT_L

13 M_B_CKE0 — U32 — MB_CKE0
13 M_B_CKE1 — U33 — MB_CKE1

13 M_B_ODT0 — AL30 — MB0_ODT0
13 M_B_ODT1 — AM32 — MB0_ODT1
AJ32 — MB1_ODT0
AM33 — MB1_ODT1

13 M_B_CS#0 — AJ33 — MB0_CS_L0
13 M_B_CS#1 — AL32 — MB0_CS_L1
AL30 — MB1_CS_L0
AL33 — MB1_CS_L1

13 M_B_RAS# — AH33 — MB_RAS_L/MB_RAS_L_ADD15
13 M_B_CAS# — AK32 — MB_CAS_L/MB_CAS_L_ADD15
13 M_B_WE# — AJ31 — MB_WE_L/MB_WE_L_ADD14

M_VREF — A19 — MB_VREFDQ

MB_ZVDDIO_MEM_S — AF32 — M_B_ZVDDIO

FP4 REV 0.93
CARRIZO-L-GP
071.FUSIN.000U
CPU BOM CTRL

MB_DATA0	A25	M_B_DQ0
MB_DATA1	C25	M_B_DQ1
MB_DATA2	C27	M_B_DQ2
MB_DATA3	D27	M_B_DQ3
MB_DATA4	B24	M_B_DQ4
MB_DATA5	B25	M_B_DQ5
MB_DATA6	B27	M_B_DQ6
MB_DATA7	A27	M_B_DQ7
MB_DATA8	A29	M_B_DQ8
MB_DATA9	C29	M_B_DQ9
MB_DATA10	B32	M_B_DQ10
MB_DATA11	D32	M_B_DQ11
MB_DATA12	B28	M_B_DQ12
MB_DATA13	B29	M_B_DQ13
MB_DATA14	A31	M_B_DQ14
MB_DATA15	C31	M_B_DQ15
MB_DATA16	E30	M_B_DQ16
MB_DATA17	E31	M_B_DQ17
MB_DATA18	G33	M_B_DQ18
MB_DATA19	G32	M_B_DQ19
MB_DATA20	C33	M_B_DQ20
MB_DATA21	D33	M_B_DQ21
MB_DATA22	G30	M_B_DQ22
MB_DATA23	G31	M_B_DQ23
MB_DATA24	J30	M_B_DQ24
MB_DATA25	J31	M_B_DQ25
MB_DATA26	L33	M_B_DQ26
MB_DATA27	L32	M_B_DQ27
MB_DATA28	H32	M_B_DQ28
MB_DATA29	H33	M_B_DQ29
MB_DATA30	L30	M_B_DQ30
MB_DATA31	L31	M_B_DQ31
MB_DATA32	AN31	M_B_DQ32
MB_DATA33	AP32	M_B_DQ33
MB_DATA34	AT32	M_B_DQ34
MB_DATA35	AU32	M_B_DQ35
MB_DATA36	AN33	M_B_DQ36
MB_DATA37	AN32	M_B_DQ37
MB_DATA38	AR31	M_B_DQ38
MB_DATA39	AT33	M_B_DQ39
MB_DATA40	AU30	M_B_DQ40
MB_DATA41	AV32	M_B_DQ41
MB_DATA42	BA33	M_B_DQ42
MB_DATA43	AY32	M_B_DQ43
MB_DATA44	AU33	M_B_DQ44
MB_DATA45	AU31	M_B_DQ45
MB_DATA46	AW31	M_B_DQ46
MB_DATA47	AY33	M_B_DQ47
MB_DATA48	BC31	M_B_DQ48
MB_DATA49	BB30	M_B_DQ49
MB_DATA50	BB28	M_B_DQ50
MB_DATA51	AY27	M_B_DQ51
MB_DATA52	BB32	M_B_DQ52
MB_DATA53	BA31	M_B_DQ53
MB_DATA54	BC29	M_B_DQ54
MB_DATA55	BB29	M_B_DQ55
MB_DATA56	BB27	M_B_DQ56
MB_DATA57	BB26	M_B_DQ57
MB_DATA58	BB24	M_B_DQ58
MB_DATA59	AY23	M_B_DQ59
MB_DATA60	BA27	M_B_DQ60
MB_DATA61	BC27	M_B_DQ61
MB_DATA62	BC25	M_B_DQ62
MB_DATA63	BB25	M_B_DQ63

M_B_DQ[63..0] 13

MB_CHECK0	N30	
MB_CHECK1	N31	
MB_CHECK2	R33	
MB_CHECK3	R32	
MB_CHECK4	M32	
MB_CHECK5	M33	
MB_CHECK6	R30	
MB_CHECK7	R31	

ECC support
MB_CHECK[7:0]
MB_DQS_H/L[8]
MB_DM[8]

For a one DIMM configuration use either M0_xx or M1_xx for these two signal groups only. Must use the same (M0 or M1) group for both CS and ODT.

SM_B_DRAMRST#

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Do Not Stuff

ED601

CZ

CZL MUA 455.04Z01.M018

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Title: FP4_DDRIII_CHB

Size	Document Number	Rev
A3	Franky_CZ/CZ-L	-3

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